UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,254	09/04/2004	Vincent Lin	VIAP0094USA	5253

27765 7590 12/28/2005

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,254	LIN ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-16* is/are allowed.

6)☒ Claim(s) *1-5,7,17-21 and 23* is/are rejected.

7)☒ Claim(s) *6 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-23 are presented in the instant application according to the Applicants' filing on 09/04/2004.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claim 8, lines 16-17, *a second logic module for performing a logic operation on the input signal and the output clock to generate the output signal* must be shown or the features canceled from the claim. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections/Minor Informalities

3. Claims 1 and 17 are objected to because of the following informalities:

Claim 1, line 6, there is already established antecedent basis for "reference clock". It is suggested that "a" be changed to -- the -- .

Claim 17, line 3, there is already established antecedent basis for "reference clock". It is suggested that "a" be changed to -- the --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> A person shall be entitled to a patent unless –

5. Claims 1-5, 17-21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Lusinchi (U.S. Patent No. 6,115,442).

With respect to claims 1 and 17, Lusinchi discloses, in Figs. 5-6, a clock circuit for generating an output clock [EQ] in a data path according to a reference clock [CLK0], in which there are signals of a plurality of periods, and each period of the signals has one rising edge and one falling edge, the clock circuit comprising a first flip-flop [10] having a first clock port, wherein the first flip-flop generates a first signal [QB] according to triggering of the reference clock on the first clock port, and the first flip-flop changes a level of the first signal when each rising edge of reference clock occurs [Fig. 6], a second flip-flop [9] having a second clock port, wherein the second flip-flop generates a second signal [QA] according to triggering of the reference clock on the second clock port, and the second flip-flop changes a level of the second signal when each falling edge of reference clock occurs [Fig. 6], and a logic module [11] for performing a logic operation on the first signal and the second signal to generate the output clock.

With respect to claims 2 and 18, Lusinchi discloses, in Fig. 6, that when the first flip-flop changes the level of the first signal at each rising edge of the reference clock, if the level of the first signal before the rising edge is a first level, the first flip-flop will change the level of the first signal to a second level after the rising edge.

With respect to claims 3 and 19, Lusinchi discloses, in Fig. 6, that if the level of the first signal before the rising edge is the second level, the first flip-flop will change the level of the first signal to the first level after the rising edge.

With respect to claims 4 and 20, Lusinchi discloses, in Fig. 6, that when the second flip-flop changes the level of the second signal at each falling edge of the reference clock, if the level

of the second signal before the falling edge is a first level, the second flip-flop will change the level of the second signal to a second level after the falling edge.

With respect to claim 5, Lusinchi discloses, in Fig. 6, that if the level of the second signal before the falling edge is the second level, the second flip-flop will change the level of the second signal to the first level after the falling edge.

With respect to claim 21, Lusinchi discloses, in Fig. 6, that if the level of the second signal before the rising edge is the second level, the level of the second signal is changed to the first level after the rising edge.

With respect to claim 23, Lusinchi discloses, in Fig. 6, that the step of generating a reference signal by using a ratio between the period of the first signal and that of the second signal before generating the output clock so that a duty cycle of the reference signal is different from that of the output clock.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lusinchi (U.S. Patent No. 6,115,442) in view of Applicant Admitted Prior Art (Fig. 2).

With respect to claim 7, Lusinchi discloses all of the claimed limitations as expressly recited in claim 1 including that the reference clock is not output from any output pad, except for a plurality of output pads to output signals of the clock circuit.

Applicant Admitted Prior Art (AAPA), Fig. 2, discloses a plurality of output pads to output signals of the clock circuit.

To configure the clock circuit of Lusinchi with a plurality of output pads to output signals of the clock circuit to facilitate implementation of different functions of digital circuits, such as adders, timers, state machines, etc. as taught by AAPA, Fig.2, would have been obvious to one of ordinary skill in the art at the time of the invention since AAPA, Fig. 2, teaches that by doing so each output port would become a transmission medium of a data path *(see Specification, pp. 2, lines 13-15 and 21-23).*

Allowable Subject Matter

8. Claims 8-16 are allowed.

9. Claims 6 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A clock circuit, in which the logic module comprises an XOR gate for generating the output clock according to results of an XOR operation between the first signal and the second signal, as called for in claims 6 and 22; and

b) A signal circuit, including a second logic module for performing a logic operation on the input signal and the output clock to generate the output signal, in combination with the remaining claimed limitation, as called for in independent claim 8.

Citation of Relevant Prior Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Verseput (U.S. Patent No. 5,535,343) discloses a method and apparatus generating write signals.

Prior art Fitch (U.S. Patent No. 5,045,715) discloses a circuit for generating stretch clock phases on a cycle-by-cycle basis.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER